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Technology for Sequential Integration of HPA and LNA on Stacked GaN Layers for 3D Packaging of Next Gen Miniaturized Power RF Transceiver Front Ends

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***Abstract*— In this work we propose a disruptive technological approach based on 3D sequential integration of high-power amplifiers (HPAs) and low-noise amplifiers (LNAs) together with RF MEMS switches. Overall scope is to enable drastic improvements in reduction of size weight and power consumption (SWaP) for next generation power RF front ends operating up to Ka band for airborne future multi-mission radars. Core of the integration concept is the stacking of a second gallium nitride (GaN) layer for the fabrication of LNA and RF MEMS switch on top of a first GaN layer with already present HPA components. The preparation of the second GaN layer is done by extreme thinning of wafers with a GaN epitaxy layer on temporary carrier wafers, followed by the permanent adhesive bonding of the thin GaN layer to the wafer with the already processed HPA components and the final release of the temporary carrier wafer from the transferred GaN layer. Bonding of silicon interposer with TSVs enables final encapsulation of the GaN stacked components and vertical signal feeding. The entire integration approach is successfully shown on 100 mm wafers with test circuits that allow subsequent electrical characterization of the signal path from the first GaN layer, through the second GaN layer as well as through the silicon interposer. The paper will discuss in detail the related technological process flow for building the 3D sequential integration stack as well as generated results such images after certain process steps, first electrical test data, considerations of thermal performance and also process improvement options.**

***Keywords*— 3D Integration, Wafer Level Packaging, Packaging of Power RF Transceiver, TSV Silicon Interposer, Wafer Bonding**

I. Introduction

Multi-mission radars (MMRs) are essential for defense in land, sea or air surveillance scenarios. Airborne radars are especially interesting for numerous applications such as anti-surface warfare, anti-submarine warfare, maritime surveillance, ground surveillance and mapping, air surveillance and support as well as detection and interception of small and low-flying aircraft or drones. [1, 2]

Most of these MMRs are based on RF front ends (RFFEs) that employ GaN technologies, which followed silicon or gallium arsenide-based systems and enabled significantly improved RF performance – greater output power, higher operating frequency, wider bandwidth and superior reliability. However, there is a continuous pressure to improve MMRs for modern defense systems, which require increased emitted power, higher frequencies and bandwidths, lower power consumption (especially in handheld devices), as well as reduced size and weight, all of which are summarized under the abbreviation SWaP. [3]

In this work we introduce a new technological approach based on 3D sequential integration of HPAs, LNAs and RF-MEMS switches towards achieving drastic SWaP improvements. In chapter 2 the integration concept is discussed in detail. Chapters 3, 4, and 5 present the first trials for implementation of the discussed technology using a simplified test layout. Goal of this work was to show the general capability

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of the technology with respect to creation of wafers with stacked GaN layers, building of TSV interposers with hermetic sealing functionality and the subsequent assembly of both types of components with reasonable electrical yield. All prototype fabrication results as well as thermal performance estimation and anaysis will be discussed and summarized in chapter 6.

II. Concept for 3D Sequential Integration

LETI [4] has initiated an ambitious 3D integration process namely 3D sequential integration (3DSI) which is the only technological option enabling the full benefits from the 3rd dimension potential thanks to its high alignment precision (σSEQ ~10 nm compared to σTSV ~0.5 µm [5]) in order to drastically increase the number of digital processors.

3DSI was used in this work employing, for the first time, GaN based MMIC FORTH technology, in order to exploit the 3rd dimension in full not to enhance the density of processors but to minimize signal losses due to the dramatic decrease in interconnects length compared to hybrid or 2D integration solutions.

Fig. 1 shows the schematic process sequence. First, HPAs are fabricated on a silicon carbide (SiC) GaN epitaxy wafer (picture A1). The second GaN layer is prepared from a different, but similar SiC GaN epitaxy wafer (picture B1). The wafer is bonded with the GaN side to a temporary carrier wafer (picture B2) and then the SiC is removed by mechanical grinding / polishing and dry etching so that only the thin GaN layer is left over (picture B3). The so called "GaN2 donor wafer" is now ready for the transfer of the GaN layer to the wafer with the HPA components. To enable this, the HPA wafer is prepared with a permanent adhesive bonding layer. (picture A2) Due to its well-known capabilities for low temperature permanent bonding with superior topography planarization, the polymer precursor Cyclotene is applied here by spin coating and subsequently bonded in a short thermo-compression type wafer bonding process to the donor wafer with the GaN2 layer. [6, 7] After a thermal cure, with transfers the Cyclotene into Benzocyclobuten (BCB), the temporary carrier wafer is removed from the back side of the GaN2 layer. (picture A3)

In the following steps LNA and RF-MEMS are fabricated on the GaN2 layer. (picture A4) During the fabrication of GaN based LNAs, a rapid thermal annealing (RTA) step at elevated temperatures is used to realize the ohmic contacts of the transistors. However, the presence of the BCB interlayer prohibits the use of RTA due to the inability of BCB to withstand temperatures higher than 300 °C. Thus, alternative approaches such as laser annealing have been employed.

In the next process sequence (picture A5) vias and metallization layers are processed for connection of the GaN1 and GaN2 layers. The vias are processed by dry etching of GaN2 and the BCB bonding layer by dry etching against a photo resist mask. As metallization Au is deposited by semi-additive processing including seed layer sputtering, lithography, electro-plating resist removal and differential etching.

The entire GaN1/Gan2 3D stack is then joined with a silicon interposer with TSVs and seal rings to ensure a hermetic encapsulation of the MEMS switches integrated on the GaN2 layer. (picture A6) The joining process is intended to be in wafer-to-wafer configuration using the well-established AuSn soldering process at Fraunhofer IZM in Berlin. [8, 9, 10] This allows later usage of the components for final assembly processes with standard AgSn based solder, which has a lower reflow temperature compared to AuSn.

The silicon interposer is ideally a simple device with TSV feed throughs in high resistivity silicon and pads for later soldering at the outside. The side for soldering to the GaN1/Gan2 stack is prepared with AuSn solder deposited by semi-additive processing. At the moment of bonding, the interposer is mounted onto a temporary carrier, which is removed afterwards.

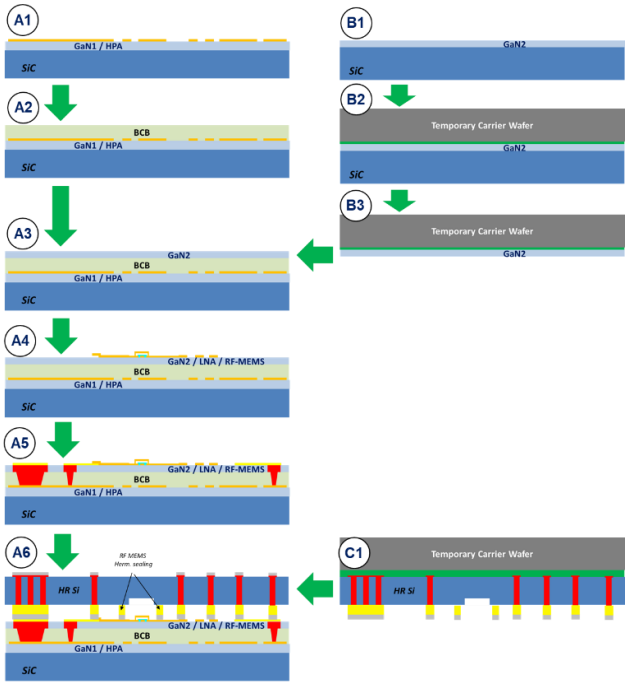

Fig. 1: schematic process flow for 3D sequential integration

III. Processing of Wafers with Stacked GaN Layers

The GaN1 wafers were prepared containing the HPAs as well as active and passive device structures using an established process at FORTH. A commercial GaN/AlGaN standard HEMT (for X-band) grown by MOCVD on (111) high resistivity silicon substrates was employed. A 10 masks set was used involving both optical as well as electron beam lithography for the realization of the 250 nm transistor gates. The footprint of HPA was 3.0 x 1.5 mm^2.

Passive devices include transmission lines, inductors and capacitors in a two-port configuration with a ground-signal-ground (GSG) pad configuration for on-wafer probing [11]. The same GSG box is used for active device characterization, with common source connected devices placed as test structures.

Both gate and drain bias signals are provided via the vector network analyzer (VNA) during later on-wafer probing.

A typical image of the fabricated structures is shown in Fig. 2. The images correspond to condition of picture A1 in Fig. 1. In preparation for wafer bonding with the GaN2 donor wafer, the fabricated structures were coated with a thin Cyclotene layer.

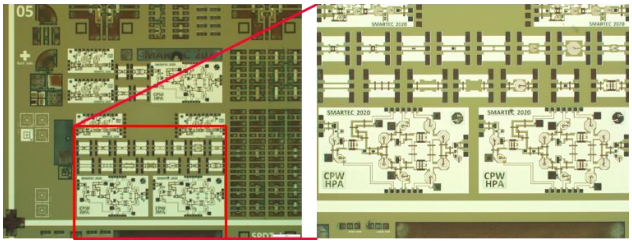

Fig. 2: HPA and RLC test structures on GaN1 wafer

In the process development for the preparation of the GaN2 donor wafer (pictures B in Fig. 1), silicon wafers with 1 µm thick GaN layer were used. The wafers were initially bonded to the temporary carrier wafers using a thin thermoplastic adhesive. After bonding, the silicon was removed by grinding and polishing. Due to lack of 100 mm dry etching capability, the silicon could not be removed completely in this work. Instead to this, an approximately 10 µm thick remaining silicon layer was kept left, before the GaN layer was reached. Fist samples revealed cracked and damaged edges of the thin remaining silicon and GaN layer on the temporary carrier wafer. After introduction of an edge trimming step from the GaN side, which was done as a first step before the wafer is temporary bonded, very good results could be obtained. The images in Fig. 3 show the thin GaN layer with 10 µm remaining silicon on the temporary carrier wafer. The light shines through, since silicon is already transparent at this thickness and the carrier wafer is also optical transparent. The right image in Fig. 3 shows the very good edge quality of the thin layer. No cracks or damages are present here.

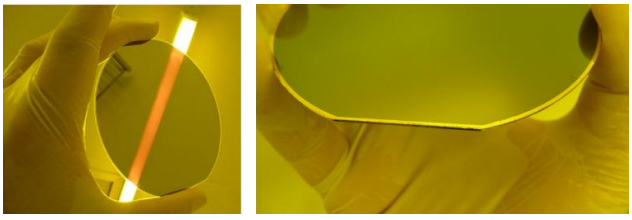

Fig. 3: GaN2 donor wafer with thin GaN layer at temporary carrier wafer

The GaN2 donor wafers were now bonded with the GaN side to the prepared test wafers with the HPA / RLC test structures and prepared Cyclotene bonding layer. The wafer bonding process was done at low pressure and moderate temperatures in the range of 150 °C. A post bond cure was applied to transform the Cyclotene into hard cured BCB. Finally, the temporary carrier wafer was removed from the GaN2 layer using a laser release process followed by an adhesive cleaning procedure.

In the next steps, photo resist lithography and dry etching processes were performed to create vias into the stack of 1 µm GaN, 10 µm Si and BCB bond layer to access the IO pads of the test structures on the GaN1 wafer. SEM images of such vias with depth in the range of 20 µm can be seen in Fig. 4. The vias were realized with an ICP etching tool employing SF6 based plasma.

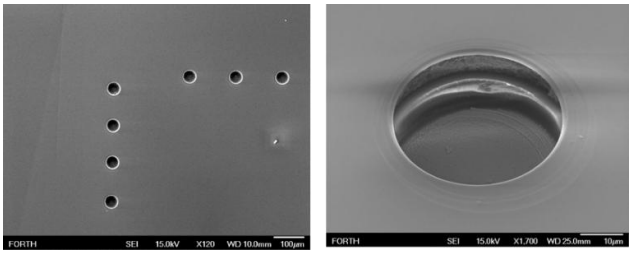

Fig. 4: dry etched vias in GaN2+Si+BCB

Finally, an Au redistribution layer (RDL) was processed by semi-additive processing to connect the IOs at the bottom of the vias and route them out to the surface of the GaN2 layer. In a further masking and electro-plating step, bumps and seal rings of Au+Sn were deposited. Both, Au RDL and Au+Sn bumps as well as seal rings are shown in the images in Fig. 5. All Au+Sn structures are later bonded with corresponding structures on the silicon interposer.

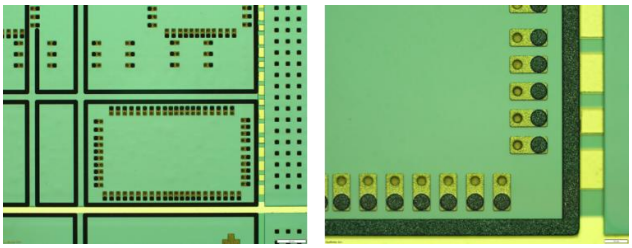

Fig. 5: RDL as well as Au+Sn bumps and seal rings processed on stacked GaN2 layer

IV. Preparation of Silicon Interposer with TSVs

The silicon interposers were fabricated using the well-established 2.5/3D integration technologies at Fraunhofer IZM in Berlin. [12, 13, 14] A typical TSV first flow was used which starts on blank silicon wafers. TSV blind holes were etched by deep reactive ion etching followed by deposition of isolation oxide, diffusion barrier and seed layer. Subsequent copper electroplating filled the blind plugs completely. The copper overburden was removed by CMP. The TSV plugs were then connected by a semi-additive structured Ni+Au metallization for final electrical probing purposes. Temporary bonding of a carrier wafer was done to allow back grind and polishing of the TSV wafer followed by TSV reveal to access the copper plugs from the wafer back side. Finally, a semi- additive process was

applied to deposit Au pads and seal rings, which are later used for soldering with the corresponding Au+Sn structures on the GaN2 layer of the wafers with the stacked GaN layers. The images in Fig. 6 show these Au features at back side of the interposers. In this state, which matches to the condition C1 in Fig. 1, the interposers are still bonded with their front side to the temporary carrier wafers.

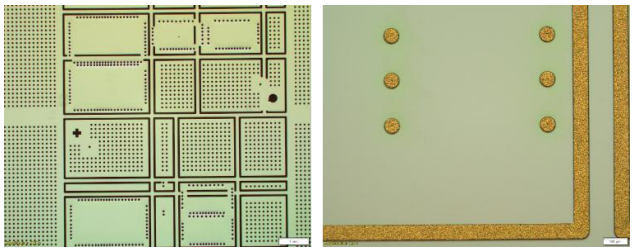

Fig. 6:Au metallization on back side view of silicon interposer

For illustration, Fig. 7 show both, an SEM as well as the corresponding EDXS composite map of the fabricated TSV interposer structure in cross section orientation. Front side Ni+Au pads, Cu TSVs as well as back side Au pads can be clearly identified here. The TSVs have a diameter of 20 µm and a depth of 90 µm. All relevant layer thicknesses of the interposers structure back annotated from the EDX analysis can also be reviewed in Fig. 8.

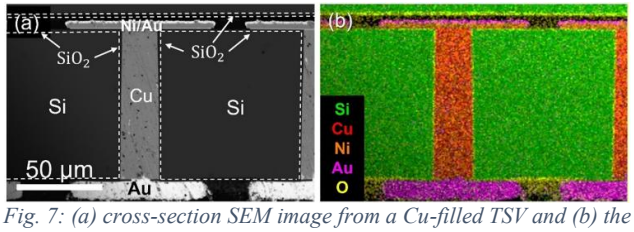

Fig. 7: (a) cross-section SEM image from a Cu-filled TSV and (b) the corresponding EDXS composite map.

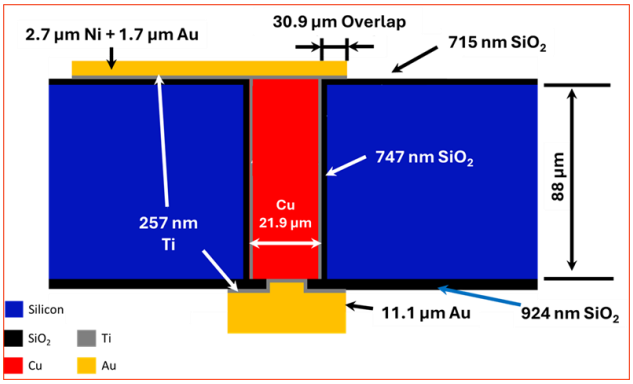

Fig. 8: cross-sectional schematic illustration of a Cu-filled TSV architecture. The experimentally measured layer thicknesses are indicated

V. Assembly of First Test Samples

For the creation of the intended 3D stack according to condition A6 in Fig. 1, the parts with the stacked GaN layers and the interposers were joined together by using an AuSn soldering process. Although the original process concept foresees the implementation of AuSn soldering of these parts by wafer-to-wafer bonding, the first samples here were bonded in die-to-die configuration. Reason for using die to die bonding was mainly to reduce risk of fail with the limited number of wafers available after the first process demonstration. To enable die-to-die bonding, both wafer types were singulated related to the two present reticle designs. The die-to-die bonding was performed by pick and place using a flip chip bonder and subsequent reflow. For secure handling and warpage prevention, the thick glass temporary carrier remained on the thin silicon interposer during flip chip assembly. This preserved flatness over the entire surface, ensuring that all thin AuSn contacts of the interposer came into contact with the substrate, not only during placement and but also during subsequent soldering. The temporary carrier is released by laser assisted debonding after the assembly process. During flip-chip bonding, the Si interposer with the thick gold pad finish was placed on the chuck, and the GaN-based component with the gold-tin solder was picked with the bonding head. Interposer and GaN based chip were first precisely aligned to each other using markers and bond structures. After placing all parts, a batch reflow was performed in a soldering oven under a protective atmosphere at a peak temperature above the AuSn20 eutectic temperature (282 °C) to ensure proper melting of the plated solder and bonding. The two reticle types were bonded successfully together, as evidenced by inspection results shown exemplary with optical and X-ray images in Figure 9.

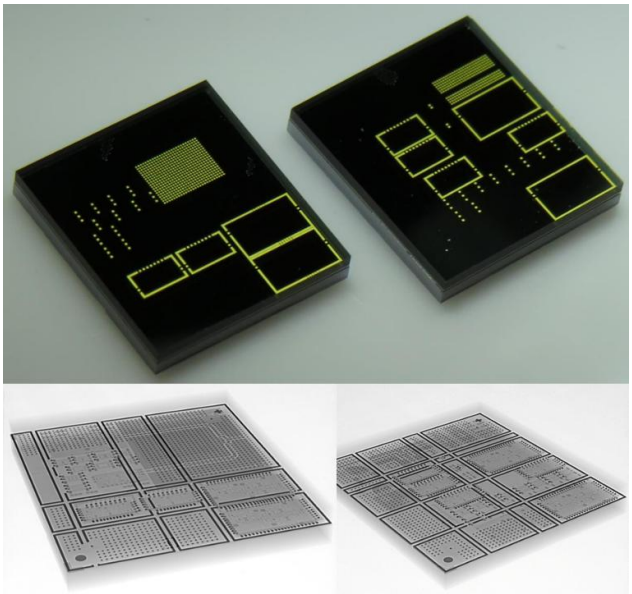

Fig. 9: optical and X-ray images of two different reticles of GaN1 and GaN2 stack bonded with silicon interposer

VI. Results

To assess the stacked 3D structure and verify the bonded parts, metallographic cross-sectioning was performed. Several planes were prepared successively to inspect different structural features, including vias in the GaN substrate, bonded I/Os, and vias in the Si interposer. Fig. 10 shows a cross-section SEM image illustrating a stacked sample consisting of the GaN stack and the bonded TSV interposer together with the indicative corresponding EDXS elemental maps of Si, Au, and Cu.

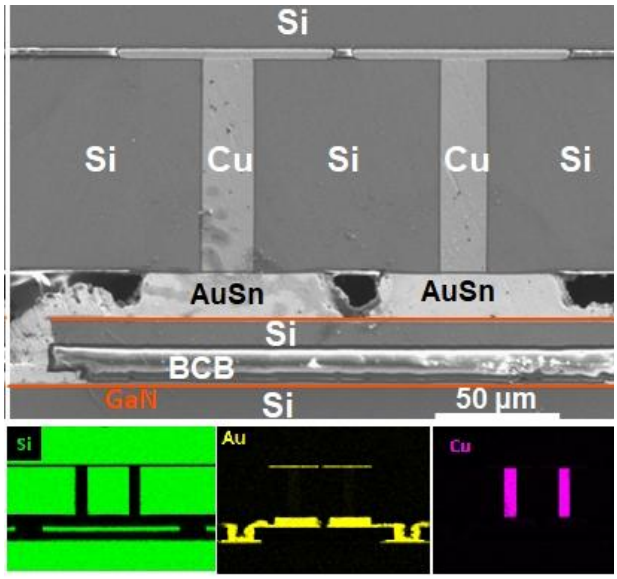

Fig. 10: cross-section SEM image presenting an overall view of the complete fabricated architecture of the GaN stacked device with the bonded TSV interposer together with the corresponding EDXS elemental maps of Si, Au, and Cu

Looking at the bottom part (GaN substrate side) of Fig. 10, the first identifiable features are the vias through the thinned silicon and the BCB bond layer to the underlying GaN layer. These vias are dry-etched and metallized with a thick gold liner deposited by electroplating. The metal layer enables electrical contacts and feedthrough from the electrical contacts of the GaN devices to the thinned silicon top surface toward the flip-chip gold bond pads. These pads are here electrically connected to the 100 µm thin silicon interposer with the AuSn solder. The bonded metal interconnects consist of thin residual gold sockets on both joined parts, with a core mainly composed of the thermally stable Au_5Sn phase and only a minimal remaining eutectic. The electrical contacts are further routed through the silicon interposer by copper-filled vias. Between the flip-chip interconnects and the copper vias, the SiO_2 passivation opening is visible. On top of the silicon, a metal layer completes the electrical path to the external side, including GSG probe pads or/and SMD pads / stud-bumping pads.

Characterization was performed to evaluate the survivability of active and passive devices, as well as the electrical continuity of the interposer to GaN1 vias. Fig. *11* presents the DC characterization setup a of HEMT while probing at the interposer level. The measured devices have a gate length of 200 nm, a gate width of 100 µm, and consists of two gate fingers. The dies were placed in MPI TS200 probe station and DC characterized using Keithley 4200 SCS parameter analyzer.

Fig. 12 demonstrates the DC characteristics of GaN1 HEMT device as measured after GaN1 and interposer level vias fabrication for V_{DS}=7 V. HEMT's threshold voltage remains the same while the saturation current and maximum g_m decreases less than 10 % after the finalization of the fabrication.

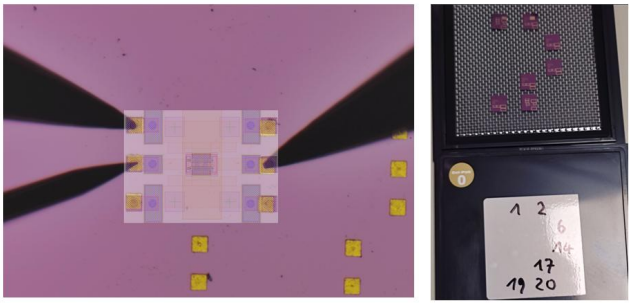

Fig. 11: (left) GaN1 HEMT device under test utilizing interposer level pads (transparent schematic added for concept) and (right) photo of characterized dies

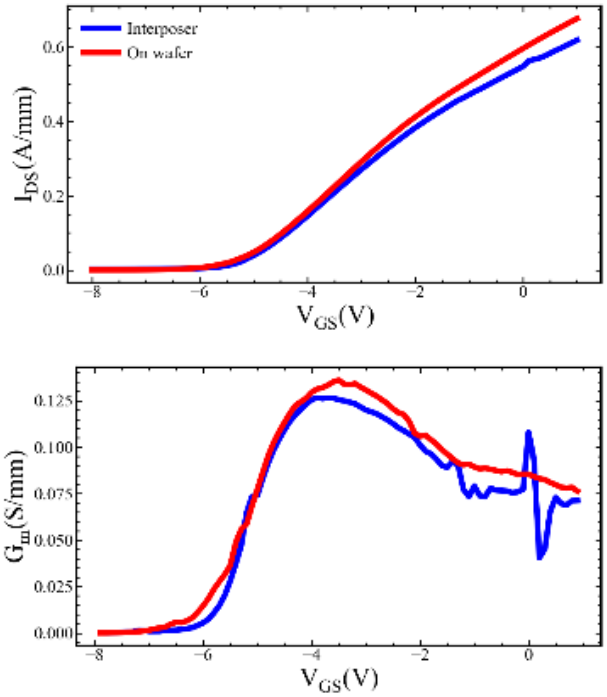

Fig. 12: (top) I_{DS}-V_{GS} (bottom) gm-V_{GS} HEMT characteristics in saturation (V_{DS}=7 V) as measured on-wafer and from interposer level.

Fig. 13: (left) photo of the die under test on probe station and (right) microscope image of a HEMT device during RF characterization.

RF characterization was conducted on passive devices-including inductors, capacitors, and transmission lines-fabricated at the interposer level using the GaN1 process (Fig. 13). The dies were placed in TS150 probe station and were characterized using Anritsu MS4644B VNA from 10 MHz to 40 GHz, while the RF pad pitch was 150 um. Key DUT parameters were extracted from these measurements, as depicted in Fig. *14* and Fig. 15.

The results confirm excellent RF continuity throughout the stack, with all devices exhibiting expected RF performance characteristics. To the best of our knowledge, this is the first demonstration of RF characterization of monolithically integrated passive devices within a GaN-on-Si 3D stack measured through the TSV silicon interposer interface.

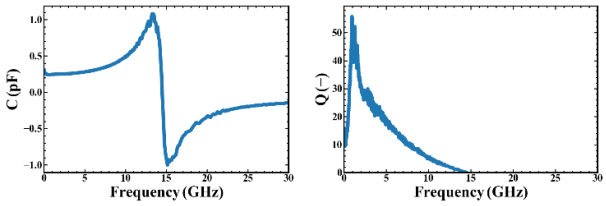

Fig. 14: capacitance and quality factor of capacitor as measured at silicon interposer level

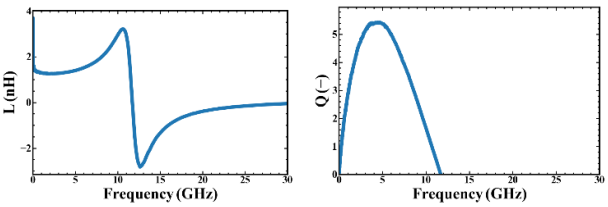

Fig. 15: inductance and quality factor of inductor as measured on at silicon interposer level

The stacked GaN integration should combine a high-power amplifier (HPA) on GaN1 with a temperature-sensitive low-noise amplifier (LNA) on GaN2, creating a fundamental thermal–RF co-design challenge. While RF performance favors close placement of the HPA and LNA, thermal considerations require minimizing heat coupling from the high-power HPA to ensure a stable LNA operating temperature. Owing to the high thermal conductivity of the SiC substrate and the backside-cooled configuration of GaN1, HPA-generated heat is expected to be predominantly extracted through the substrate toward the heat sink, thereby limiting vertical heat propagation toward GaN2.

Fig. 16 shows schematic of stack up the of the package simplified for the thermal management investigation. To validate the thermal performance, finite element (FE) simulations and thermal experiments were conducted using thermal test vehicles (TTVs) designed and fabricated to mimic the real package. The TTVs consist of two thermal test chips (TTCs) assembled on a printed circuit board (PCB).

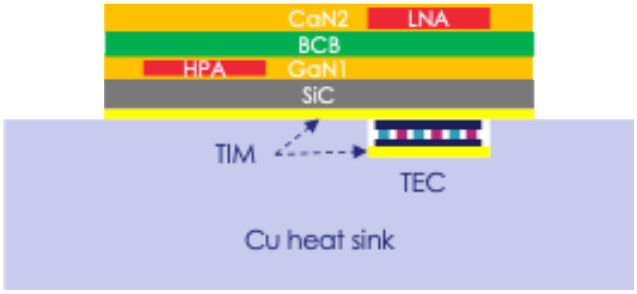

Fig. 16: simplified schematic of 3D stacked package

The upper chip (TTC2) was bonded onto the PCB using a thermally conductive epoxy and electrically connected via wire bonding. Subsequently, the lower chip (TTC1) was mounted onto the PCB through a standard solder reflow process.

The upper TTC (TTC2), representing LNA, contains ten heater tracks and a central temperature sensor [15]. The lower TTC (TTC1), representing the HPA, comprises four unit cells, each including two heaters and one central temperature sensor. Both TTCs can be powered up to 10 W/mm². The FR4 substrate is thermal equal to the BCB bonding layer between GaN1 and GaN2 in the real package.

To investigate the effect of the thermoelectric cooler (TEC) as a temperature stabilizer for the LNA, two TTV variants were realized: one without TEC and one with TEC, as shown schematically in Fig. 17 and Fig. 18.

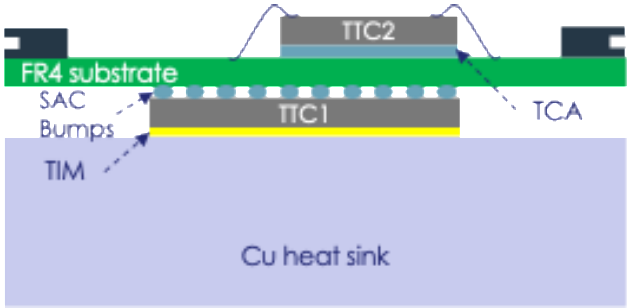

Fig. 17: concept of the thermal test vehicle w/o TTC

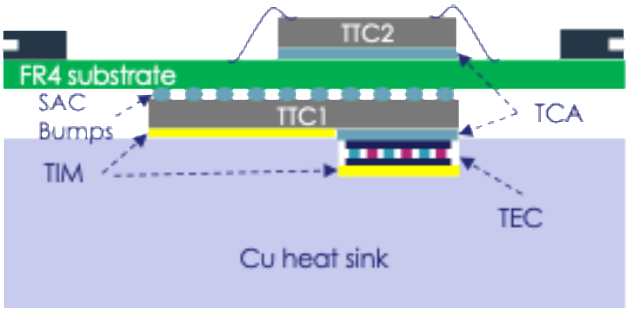

Fig. 18: concept of the thermal test vehicle w/ TTC

Finite element simulations were performed to evaluate the feasibility of actively cooling the assembly using a thermoelectric cooler (TEC). The objective was to assess whether integrating a TEC module between the device stack and the heat sink could reduce the operating temperature of the low-noise amplifier (LNA) compared to the baseline passive-cooling configuration.

Two steady-state simulations were conducted: one with TEC (w/ TEC) and one without TEC (w/o TEC). Both models included TTC2 representing the LNA, TTC1 representing the HPA, thermal interface materials, and a heat sink.

The simulation results indicate that incorporating the TEC did not provide any measurable improvement in cooling performance. In fact, the average LNA temperature increased slightly from approximately 27.86 °C in the w/o TEC configuration to 28.50 °C in the w/ TEC configuration. (Fig. 19)

Based on these findings, the required TEC cooling capacity to match the performance of the w/o TEC configuration was estimated. The analysis suggests that the TEC would need a cooling capacity of at least 23.5 W within its operating range to achieve parity with or outperform the passive-cooling concept.

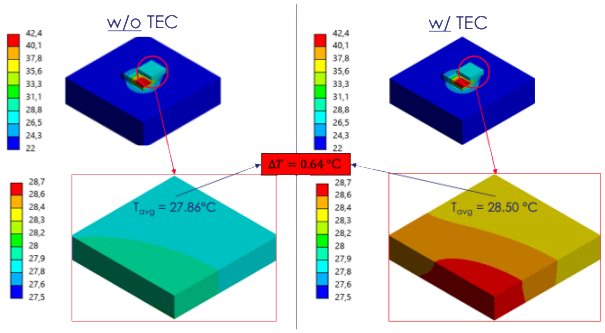

Fig. 19: thermal simulations results with and without TEC

The thermal behavior of the package was investigated using the thermal test vehicles described above. The package was mounted onto a copper heat sink plate with an area of 100 mm2 and a thickness of 60 mm, featuring a milled cutout to accommodate the TEC. The TTV was powered and monitored using a dedicated TTV control unit.

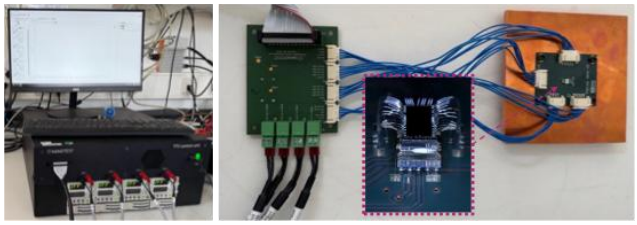

Fig. 20: measurement setup for thermal behaviour

To verify the functionality of the TEC, the temperatures of both TTCs were measured at P_{TEC} = 0 W and P_{TEC} = 2 W, A temperature reduction of approximately 5.2 K was observed when the TEC was activated. In a second step, TTC1 (HPA) was powered at 1.5 W while TTC2 remained off. The temperatures of TTC1 and TTC2 were monitored at different TEC power levels (P_{TEC} = 0, 2, 4, 6 and 10 W). The results did not show a positive effect of the TEC on either the HPA or LNA temperatures. The following graphs present the temperature of TTC1 (HPA) and TTC2 (LNA) at different TEC power levels.

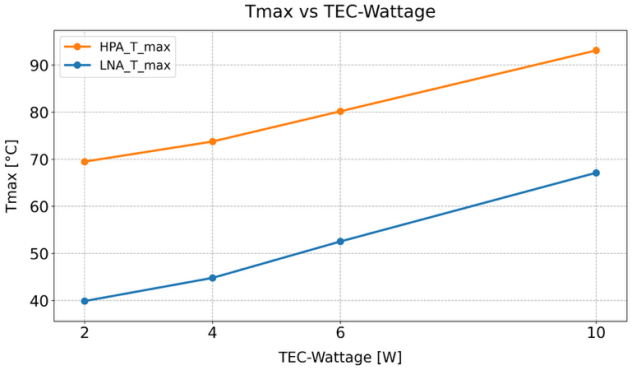

Fig. 21: HPA and LNA temperature at different power levels of the TEC

For comparison, measurements were also performed on the TTV without a TEC. These tests were conducted using the same copper cooling plate and identical thermal interface material (TIM). The results indicate improved cooling performance when the package is directly attached to the heat sink. It turned out that the temperatures in both, TTC1 (HPA) and TTC2 (LNA) were below 45 °C when TTC1 is powered by 1.5 W.

Experimental results from both test vehicles show good agreement with the thermal simulation predictions. However, the measurements further indicate that the TEC used in this study is not suitable for effective temperature stabilization of the LNA. Therefore, a TEC with a higher maximum heat pumping capacity (Qmax) is required to achieve adequate thermal regulation.

CONCLUSION AND OUTLOOK

The concept of 3D sequential integration (3DSI) of HPAs and LNAs was successfully demonstrated in this work as general fabrication approach for next generation of power RF front ends. 100 mm wafers with stacked GaN layers were created by utilizing temporary wafer bonding of wafers with GaN epitaxy layer, removal of their bulk substrate as well as subsequent transfer bonding of the remaining thin GaN layers to other wafers with GaN epitaxy layer and already fabricated test structures. Core elements of this technology are (1) the temporary and permanent wafer bonding processes for preparation and transfer of the thin GaN layer, (2) the via formation and metallization processes for the connection of the stacked GaN layer as well as (3) the connection and sealing of the GaN stack by a TSV interposer. All these three core processes could be implemented successfully in this work. RF measurements of inductors and capacitors implemented at the first GaN layer have shown continuity and expected electrical behavior measured the gingal paths though vias in the stacked GaN layers as well as through the TSVs of the silicon interposer.

Thermal simulations and measurements of the new package types based on 3DSI have revealed high sensitivity and necessity for efficient back side cooling of the lower GaN layer with the heat dissipating HPAs as well as a positive effect of the BCB used for permanent bonding of the upper GaN related to thermal decoupling of heat sensitive LNAs implemented in the upper GaN layer.

In the next phase of the project a real power RF module will be fabricated using the developed technology. Planned is the integration of HPA at the first GaN layer and the integration of LNA and RF-MEMS switch at the second GaN layer.

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