Showcase of the first GaN HPA tape out: Technology, PDK, design and fabrication in Greece

Nikolaos Makris[1,2,*], Evangelos Aslanidis[1,2,*], Antonios Stavrinidis[1,2], George Stavrinidis[1,2], Athanasios Kostopoulos[1,2], George Konstantinidis[1,2], Giannis Kontogianopoulos[3], Paolo Fioravanti[3], Lefteris Sarris[3], Errikos Lourandakis[3], Paolo Martins[4] and Afshin Ziaei[4]

[1]Foundation for Research & Technology - Hellas (FORTH), Inst. Electronic Structure & Laser, Heraklion, Greece

[2]Department of Physics, University of Crete, Heraklion, Greece

[3]Circuits Integrated Hellas, Leof. Kifisias 226, 14562 Kifisia, Attica, Greece

[4] Thales Research and Technology, Palaiseau, France

*nmakris@iesl.forth.gr, *e.aslanidis@iesl.forth.gr

In this work, we present the first end-to-end GaN MMIC design-to-fabrication activity in Greece. FORTH developed a 200nm GaN HEMT in-house process design kit (PDK) in collaboration with CIH. The PDK was used for design and simulation of a two-stage GaN HPA for X-Band applications. The MMIC layout was provided to FORTH for final check, full wafer design and in-house fabrication.

The flow of this work is demonstrated in fig. 1. Initially, FORTH performed several iterations regarding technology optimization and process calibration. Ohmic contacts (i.e. different RTA conditions, GaN n+ regrowth), EBL gate definition and SiN passivation (i.e. investigation of the effect different SiN stoichiometry passivation) were subjects of extensive investigation and optimization. RF HEMT test runs were fabricated for assessment and model parameter extraction (fig.2). FORTH GaN HEMT PDK was developed in collaboration with CIH and provided HEMT schematic and layout PCell. The simulations were based on a customized parameter set of ASM HEMT model[1] (fig. 3). Scripting language was used to provide automatic HEMT layout design based on user input parameters and FORTH technology design rules.

The MMIC was designed by CIH, employing a two-stage cascade differential amplifier with 50Ω I/O loads and balun feed. The differential HEMT pair with balun feed provides high stability, high power density and easier DC supply and decoupling. The HPA output power saturates at 1W (30dBm) around 10GHz with a 15% fractional bandwidth (fig. 4).

Following post-layout simulations, HPA's design was provided to FORTH for fabrication. Firstly, HEMT mesa were formed followed by RTA for ohmic contact formation. 100nm SiN passivation was deposited. Resistors were patterned and 100nm of TaN was deposited. The gate foot and head were formed by EBL followed by gate metal deposition. Second 300nm SiN layer was deposited. After this step, 1um thick gold layer is deposited to form HEMT electrodes. 250nm SiN is deposited as capacitor dielectric. Finally, SiN on device electrodes and vias is etched and air-bridges are formed using electroplating.

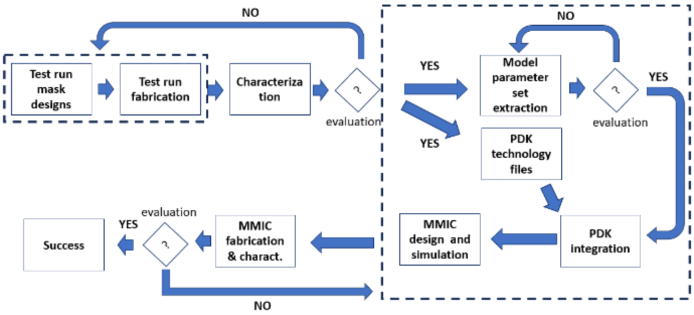

Fig.1: Schematic of work flow

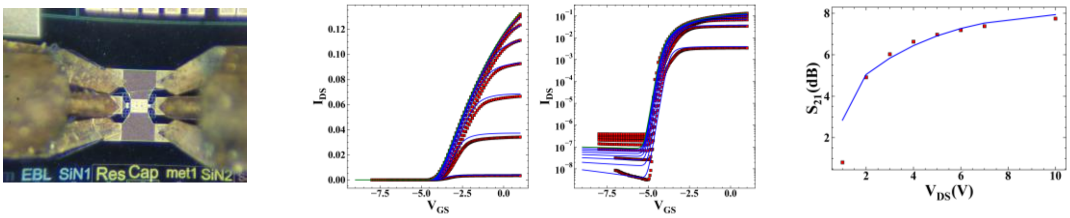

Fig.2: microscope image of DUT(left), I-V(center) and S_{21} vs V_{DS} (right)@V_{GS}=-3.5V,10GHz

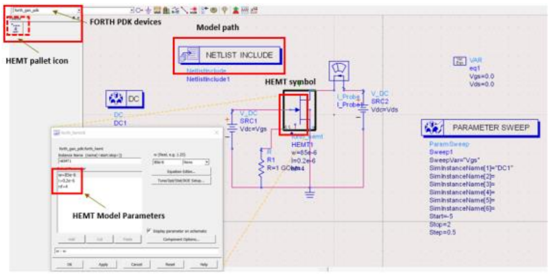

Fig.3: HEMT schematic view

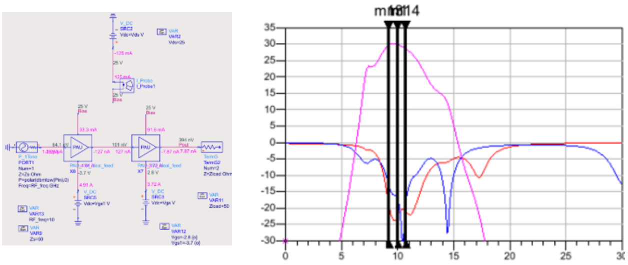

Fig.4:FORTH GaN HPA schematic (left) and Simulated S11,S12,S21,S22 vs freq. (left)

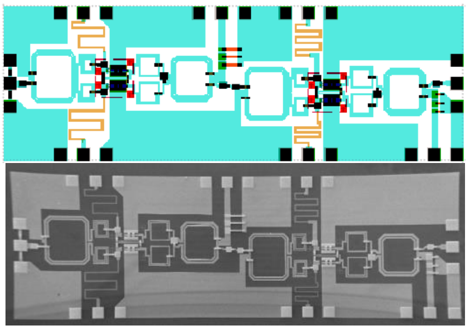

Fig.5: FORTH GaN HPA layout(top) and SEM image as fabricated (bottom)

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[1] S. Ghosh, S. A. Ahsan, A. Dasgupta, S. Khandelwal and Y. S. Chauhan, "GaN HEMT modeling for power and RF applications using ASM-HEMT," *2016 3rd International Conference on Emerging Electronics (ICEE)*, Mumbai, India, 2016, pp. 1-4, doi: 10.1109/ICEmElec.2016.8074569