

Heterogeneous AiP/SiP for Satcom

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Abstract

This paper presents Circuits Integrated Hellas's (CIH) innovative use of III-V compound semiconductors with advanced 3D packaging. CIH introduces disruptive, high-performance solutions for satellite communication (SatCom) applications, leveraging System-in-Package (SiP) and Antenna-in-Package (AiP) methodologies. These approaches minimize the weight, volume, and cost of flat-panel phased array antennas, addressing a critical need in modern space communications infrastructure and providing a unique competitive edge.

INTRODUCTION

The rapid expansion of global satellite communication (SatCom) systems [1],[2], especially with the growing deployment of Low Earth Orbit (LEO) satellite constellations, has created an urgent need for advancements in antenna technology. Flat Panel Phased Array Antennas (FPPAs) are critical for delivering reliable, high-speed connectivity, but current designs relying on discrete, bulky components present significant challenges in scalability, cost, and efficiency. Circuits Integrated Hellas (CIH) has developed a groundbreaking approach to address these limitations by integrating III-V compound semiconductors with silicon technologies within a unified 3D package [3]-[5]. CIH's product roadmap combines the distinct advantages of compound III-V and silicon technologies [6], enabling unprecedented levels of miniaturization, cost reduction, and performance optimization. By integrating components like power amplifiers, phase shifters, and splitters within a compact System-in-Package (SiP) and Antenna-in-Package (AiP) configuration, CIH achieves a high degree of functionality in a minimal footprint. This innovative integration achieves a significant breakthrough in system-level efficiency, making CI III-V technology a leading choice for next-generation SatCom applications.

A comparative analysis in Fig. 1 highlights the performance and cost benefits of CIH's approach. To read the data provided in Fig. 1, we assume a single patch antenna element of approximately Gain=6dBi, which is a typical value for microstrip patch antennas. The antenna array will exhibit a theoretical gain $G_{array}=10 \cdot \log_{10}(\#elements \cdot 10^{G_{gain}/10})$ expressed in dBi. For example, when targeting an Effective Isotropic Radiated Power (EIRP) of 49dBW, which is typical for a good uplink connection, we may formulate the total RF power needed from the antenna array as follows:

$$RF_{power(dBm)} = EIRP_{(dBW)} + Losses_{(dB)} + 30 \quad (1)$$

From the generated total RF power of the array, we may calculate the power associated with the power amplifier (PA) circuitry as follows.

$$PA_{power(dBm)} = RF_{power(dBm)} - G_{array(dBi)} \quad (2)$$

$$PA_{element(W)} = \frac{10^{(PA_{power(dBm)}/10)}}{1000} / \#elements \quad (3)$$

$$PA_{element(dBm)} = 10 \cdot \log_{10} \left(\frac{PA_{element(W)}}{1mW} \right) \quad (4)$$

Some insertion loss is accounted for in the power splitting network that feeds the antenna array and here we assume an insertion loss of 2.5dB for this exercise. In Fig. 1 the calculated RF power per array element (4) is presented over the total number of elements for the antenna array.

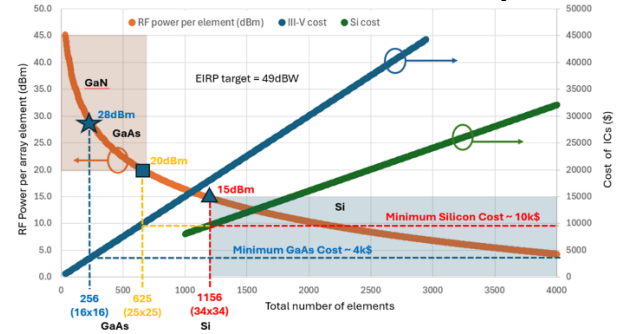


Fig. 1. Comparison between III-V & Si technologies for the design of phase array antennas at EIRP=49dBW.

A traditional silicon-based array requires a 34x34 element configuration at 15dBm per element, while an equivalent GaAs III-V enabled array achieves the same performance with just 25x25 elements at 20dBm each, reducing the area by approximately 54%. Further optimization of the III-V parts reduces this area to 16x16 elements at 28dBm, or about 22% of the silicon-based area, at a cost 40% lower than the silicon solution. The combined use of III-V [7],[8] and silicon in the CI III-V roadmap positions CIH to disrupt the SatCom market, delivering a high-performance, cost-effective antenna technology [9],[10] tailored for the demands of modern satellite systems. By addressing industry needs for lighter, more compact, and efficient antennas, CIH's CI III-V product

line establishes a new benchmark in SatCom integration and performance, enabling the unprecedented mixture of performance and flexibility. The high level of integration of components typical of beam forming systems (power amplifier, splitter, combiner, antenna, phase shifter, etc.), combined with high efficiency, unprecedented, optimized miniaturization, and cost reduction without compromising performance, makes CI III-V technology best-in-class.

TECHNICAL OVERVIEW OF CIH APPROACH

To achieve the integration levels required for flat panel antennas, CIH's design approach departs from traditional compound III-V distributed components, favoring lumped passive components with improved Back-End-Of-Line (BEOL) capabilities [11],[12]. Additionally, Through-Semiconductor Vias (TSVs) are employed to enable low-loss, low-inductance RF routing off the chip [13]. CIH's designs balance area optimization with performance retention, supported by TSV-enabled processes and air-bridge transitions. Figure 2 demonstrates a wafer level chip scale package (WLCS) transition experiment designed by CIH based on a GaAs process with TSV RF transitions. As can be seen from the de-embedded measurements, where the electrical reference plane is moved right below the TSV transition on the printed circuit board (PCB) level, the insertion loss of a THRU transition is below 0.2dB up to Ka-band frequencies. As a result, we can calculate a single TSV transition from the GaAs chip through the substrate as a low loss RF transition with an industry leading insertion loss of only 0.1dB. The TSV transitions [14],[15] allow for an industry leading footprint which provides low loss and allow for DC & RF signal routings through the semiconductor substrate. As a result, a packaged surface mount device (SMD) is obtained as shown in Fig. 2.

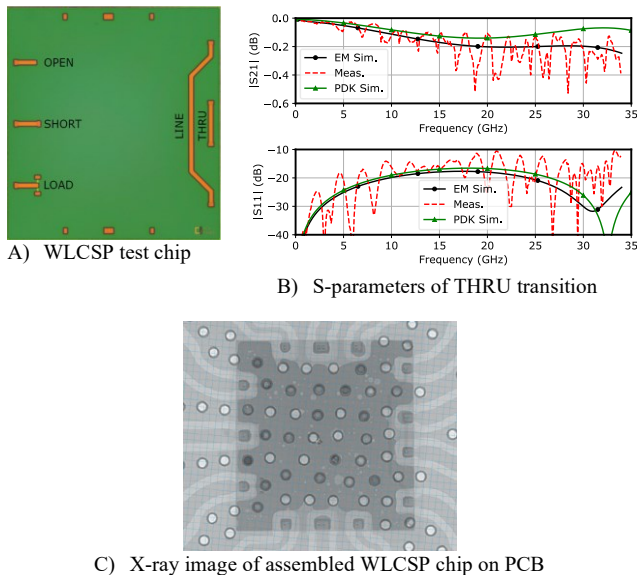


Fig. 2: GaAs wafer level chip scale package (WLCS) experiment

Additionally, CIH designed an experiment on the same GaAs process with passive devices with an industry standard single metal back-end-of-line (BEOL) process with air-bridge transitions, as shown in Fig. 3. CIH was able to demonstrate balun designs in a single metal plus air-bridge BEOL process and demonstrate impedance transformation capabilities by achieving different inductance ratios at the single-ended and differential coils of the designed baluns. All passive devices were characterized by an on-wafer probe tip calibration [16] and consecutive open-short de-embedding structures for both the primary and secondary coils.

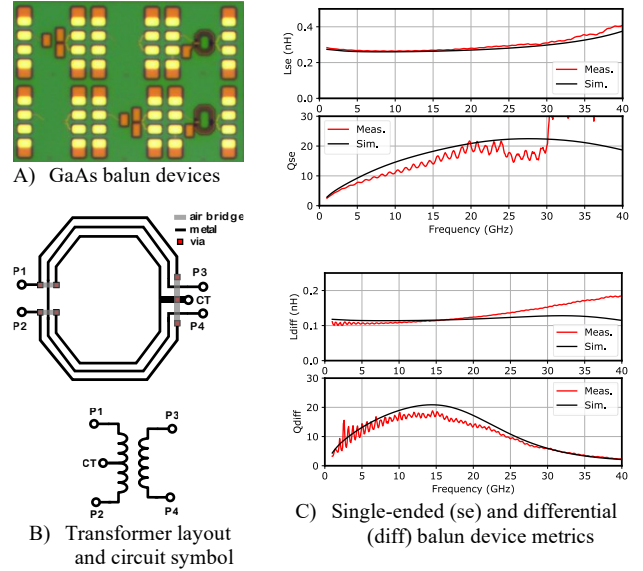


Fig. 3: GaAs wafer with passive device experiments.

Based on the above shown RF transitions and passive elements, CIH designed a differential unit amplifier based on mix between transformer based and distributed passive component design that minimizes area with minor loss of performance. In Fig. 4 an assembled GaAs PA test chip is given along with the experimental results of a single amplifier unit targeting an output power of >26dBm.

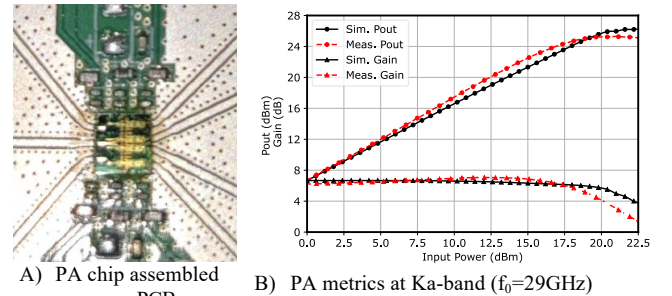


Fig. 4: Fabricated GaAs WLCS PA soldered on PCB for RF measurements with co-axial connectors.

Figure 4 shows correlation between measured and simulated results for a single GaAs PA unit including PCB-die-PCB transitions. The entire 12.5mm² GaAs PA chip when designed

as a multipath amplifier with various such PA units in parallel can host up to 4W (36dBm) in output power at P_{1dB} compression. Based on this approach, CIH has a patent pending dual output power amplifier (PA) topology that is currently been optimized for Ka-band AiP deployment. The entire wafer level chip scale package solution comes with a minimum and industry leading footprint overhead and as a molded chip solution with a thermal resistance of approximately 3K/W. The molded and packaged III/V PA module is easily soldered onto any flat substrate by its backside pin pattern supporting both RF and DC signal connections.

3D HETEROGENEOUS AiP/SiP INTEGRATION

CIH is able to design performant III-V components that fit the $\lambda/2$ array, where λ the free space wavelength, required in flat panel antennas at uncompromised performance. This unique capability is at the core of the 3D heterogeneous integrations that CIH is targeting in its development roadmap. CIH's solution involves the integration of high-performance compound semiconductors (III-V) such as GaAs and GaN with Silicon (Si) substrates in a 3D configuration, creating a unified, compact SiP/AiP structure, under the Kythron platform shown in Fig. 5.

This architecture optimizes components like power amplifiers (GaAs), phase shifter/beamformer (Si), and low-noise amplifiers (GaAs) for high-frequency and high-power performance by implementing a complex SiP/AiP RF module for transmit (Tx) and receive (Rx) operation. Indicative performance metrics of such a Tx/Rx module based on the Kythron platform are summarized in Tab. I.

TABLE I – CALCULATED KYTHRION Tx/Rx MODULE METRICS

Rx (GHz)	Tx (GHz)	EIRP (dBW)	G/T (dB/K)	Array Size	Module Size (mm ²)
17.7-20.2	27.5-30	23	-4.5	2x2	10x10
		60	13.5	16x16	80x80

To understand the benefits of the proposed heterogeneous 3D IC integration proposed by CIH, a conceptual diagram of a 2x2 unit cell is given in Fig. 6. Such a 2x2 unit design can be used in a modular approach to implement the needed phased array sizes as given in the analysis of Fig. 1. The shown module implements a beamforming function with a silicon IC die for the antenna array [17] and a patent pending selective right/left hand polarization selection implemented by the III/V amplifier circuitry and a dual-polarized flat antenna design, where individual Tx and Rx antenna patches are stacked on top of each other. As a result, the Kythron platform allows for an extremely compact and functional transmit and receive module suitable for deployment in larger flat panel array applications.

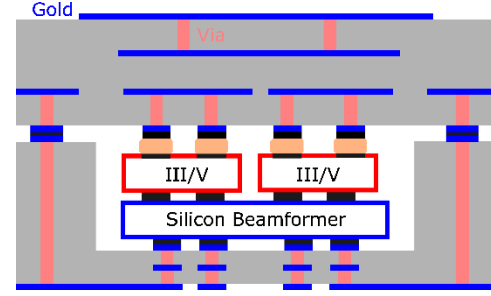


Fig. 5: Example cross section of CIH Kythron 3D IC heterogeneous SiP/AiP architecture.

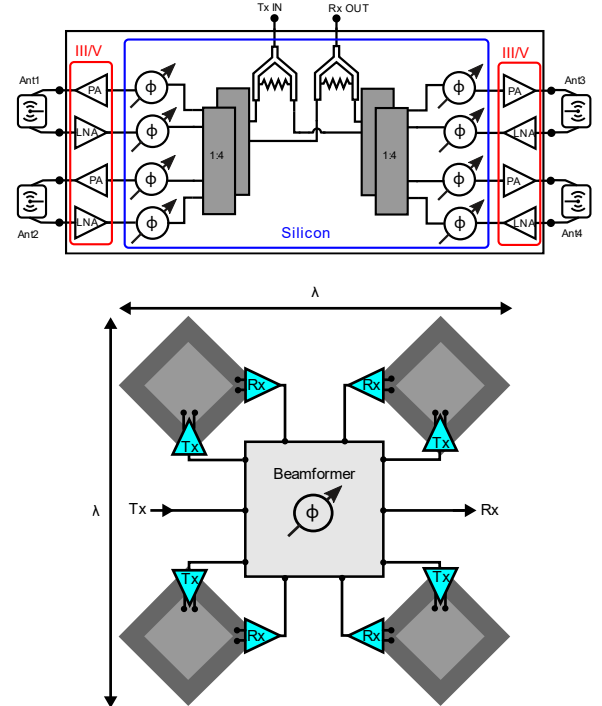


Fig. 6: Architecture and conceptual top view of 2x2 flat antenna array unit based on the CIH Kythron platform for Tx/Rx duplex SatCom links. The dimension of the above configuration is 10mm x 10mm for Ka-band Rx/Tx deployment (drawn not to scale).

IMPACT ON SPACE SEGMENT SATCOM

CIH's approach to integrating Flat Panel Phased Array (FPPA) antennas in a compact 3D configuration provides a significant advantage in terms of weight reduction, which has a direct impact on payload costs for Low Earth Orbit (LEO) satellites. By reducing FPA weight by 60%, CIH's technology enables cost savings of approximately \$40,000 to \$60,000 per satellite, depending on the configuration. These numbers are estimated using minimum published cost to orbit (Falcon Heavy), presently ranging from 1500\$ to 38000\$ per kilogram depending on the vector [18].

This weight reduction not only lowers the overall launch costs but also allows satellite operators to increase payload

capacity, potentially adding more functional systems or additional satellites in a single launch. Furthermore, lighter satellites extend service lifetimes by minimizing wear from atmospheric drag, which is especially beneficial in LEO where satellites typically need replacement every five years. Thus, CIH's approach enhances cost-efficiency and operational flexibility, expanding the revenue potential for service providers deploying high-speed, low-latency broadband constellations in LEO.

CONCLUSIONS

CIH's pioneering use of III-V semiconductors in a 3D integrated package sets a new standard in phased array antenna technology. By achieving high performance at reduced costs, CIH's innovation broadens space-based communication capabilities, promising to drive broader SatCom coverage and accessibility. Next future plans include the release of advanced 2x2 AiP units enabling dual beam transmit and receive beamforming implementations at less than half the cost, weight and area than current solutions.

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ACRONYMS

AiP: Antenna in Package
 BEOL: Back-End-of-Line
 DC: Direct Current
 EIRP: Effective Isotropic Radiated Power
 FPPA: Flat Panel Phased Array Antennas
 G/T: Gain over Temperature
 LEO: Low Earth Orbit
 MMIC: Microwave Monolithic Integrated Circuit
 PA: Power Amplifier
 PCB: Printed Circuit Board
 RF: Radio Frequency
 SatCom: Satellite Communication
 SiP: System in Package
 SMD: Surface Mount Device
 TSV: Through Semiconductor Via
 WLCSP: Wafer Level Chip Scale Package